

Conference Program



6th Conference on Ph.D. Research in
Microelectronics & Electronics

PRIME 2010

*18 – 21 July 2010 Berlin Institute of
Technology, Germany*

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Sessions Matrix – Prime 2010

Time	Mo, 19.07.2010		Tue, 20.07.2010				Wed, 21.07.2010		
	MA041	MA043	MA041	MA043	MA141	Foyer, 1 st Floor	MA041	MA043	MA141
08:30-10:10	Plenary Session		EU ECTS Initiative Company Presentations				Session 14 Transceivers	Session 15 Digital and Low Power Circuits	Workshop Ansys
10:10-10:40	Coffee/Tea		Coffee/Tea				Coffee/Tea		
10:40-12:20	Session 1 Sensor Systems 1	Session 2 Analog and Mixed Signal Circuits 1	Session 7 Low Noise Amplifiers	Session 8 Image Processing	Workshops R&S, CST		Session 16 Frequency Synthesizers	Session 17 VLSI	
12:20-13:40	Lunch		Lunch				Lunch		
13:40-15:20	Session 3 Sensor Systems 2	Session 4 Analog and Mixed Signal Circuits 2	Session 9 Power Amplifiers and Power Devices	Session 10 Analog and Digital Signal Processing	Workshop Agilent		Session 18 Frequency Generation/ Conversion Circuits	Session 19 Sigma Delta Modulators	
15:20-15:50	Coffee/Tea		Coffee/Tea				Closing Session, Award Ceremony (MA041)		
15:50-17:30	Session 5 Sensor Systems 3	Session 6 Data Converters	Session 12 Device Technology and Passives	Session 13 Computer Aided Design		Session 11 Poster Session			
	Prime Welcome Reception (17:30, Foyer – 1 st Floor)		Prime Boat Trip – Berlin City Tour (Departure: 20:00, Salzufer)				PRIME  2010		

Registration opens Monday, 7:30 am

Conference Organizers

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Verein der Freunde der Hochfrequenztechnik der TU Berlin

Exhibition Organizer



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Welcome Message from the General Chairs

On behalf of the whole organization committee we would like to welcome you to the PRIME 2010 conference in Berlin. PRIME 2010 will take place in the western heart of Berlin at Berlin Institute of Technology. PRIME has been established over the recent years as an important conference where in particular PhD students can present their project results and can get in contact with people from the industry. The organization committee has worked out a diversified conference program. Besides of the paper sessions a company exhibition and workshops have been organized. This year, almost one hundred papers have been accepted for oral and poster presentation. Best papers will be distinguished by the traditional PRIME Leaf Certificates which will be awarded on Wednesday afternoon.

The conference program starts on Monday morning with the opening session followed by two renowned invited speakers, Dr. Christoph Kutter from Infineon Technologies, Germany, and Professor Sayfe Kiaei from the Arizona State University, USA. A comprehensive technical program featuring 18 technical sessions, one poster session, and workshops given by leading companies follows from Monday to Wednesday. In a special "company representation session", international microelectronics companies will introduce themselves, their technical working fields and job offers.

On the social event side the conference reception will take place on Monday evening. A particular highlight will be the boat tour on Tuesday evening through the city center of Berlin. During the boat ride the gala dinner will take place.

We would like to thank particularly all our sponsors for their support. Thank is given also to the Technical Program Committee, the Steering Committee, the paper review board and to all session chairmen for making this conference possible. And last but not least, our conference secretaries Felix Gölden, Daniel Gruner and Viswanathan Subramanian who deserve a special mention for their countless efforts in making PRIME 2010 a success.

We appreciate all presentations from the invited speakers contributing speakers and participants in making this conference to an inspiring and motivating event with many stimulating discussions with participants, colleagues and friends.

We would like to take this opportunity to thank the German VDE/ ITG as the responsible organizer and to the IEEE in supporting the conference with technical co-sponsorship. We are looking forward to making the 6th PRIME conference a successful and exciting event.

See you in Berlin!

Georg Böck and Frank Henkel

General Chairs

PRIME2010

PRIME 2010 - Team

Conference Chairmen

Georg Böck, Technische Universität Berlin, Germany

Frank Henkel, IMST GmbH, Germany

Conference Secretaries

Daniel Gruner, Technische Universität Berlin, Germany

Viswanathan Subramanian, Technische Universität Berlin, Germany

Felix Gölden, Technische Universität Berlin, Germany

PRIME Steering Committee

Franco Maloberti, University of Pavia, Italy (Chairman)

Andrea Baschiroto, University of Lecce, Italy

Catherine Dehollain, EPFL, Switzerland

Alberto Gola, Infineon, Italy

Frank Henkel, IMST GmbH, Germany

Wolfgang Pribyl, Graz University of Technology, Austria

Peter Kennedy, University College Cork, Ireland

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John Gerrits	Vittorio Ferrari
Kari Halonen	Wolfgang Pribyl
Khodabandehloo Golnar	Yihui Chen
Manfred Glesner	Zhipeng Ye

Exhibitors

Rohde & Schwarz

Computer Simulation Technology (CST)

ANSYS

IMST GmbH

Agilent

Broadcom Netherlands B.V.

PRIME 2010 – Venue

Technische Universität Berlin

Mathematics Building (MA)

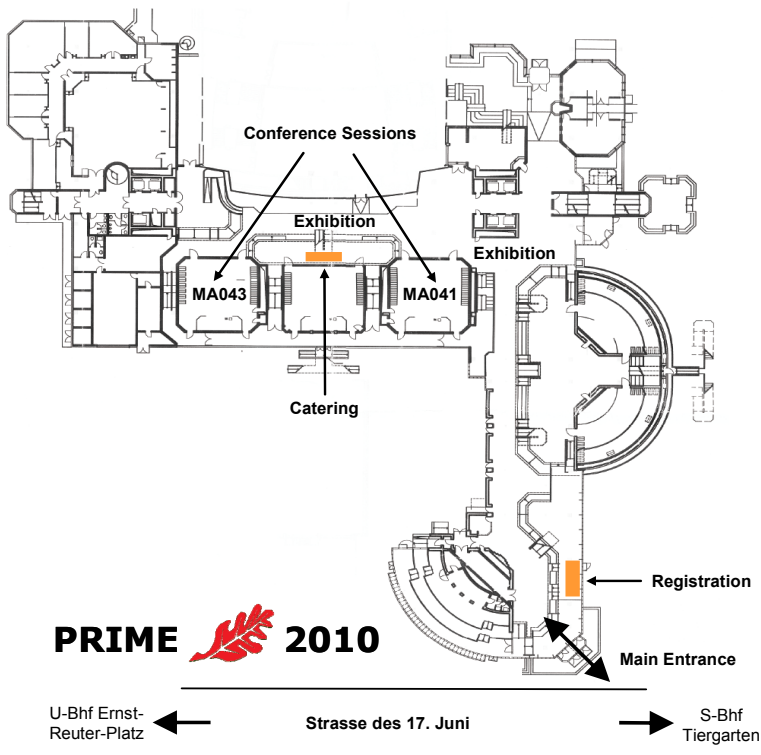
Straße des 17. Juni 136

10623 Berlin, Germany

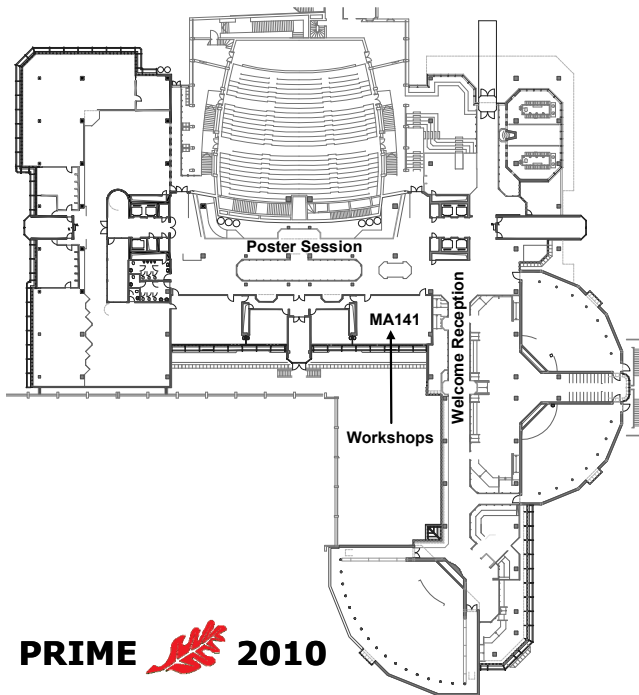
PRIME 2010 will be held at Technische Universität Berlin, Straße des 17. Juni 136, 10623 Berlin. It is located in the western heart of the city, in Charlottenburg close to Zoologischer Garten, Kurfürstendamm, Gedächtniskirche, and Siegestsäule.

PRIME 2010 will take place in the Mathematics (MA) Building that has its main entrance from Strasse des 17. Juni, only two minutes walk from U-Bahn Station Ernst-Reuter-Platz or S-Bahn Station Tiergarten.

Floor Plan – Ground Floor



Floor Plan – First Floor



PRIME  **2010**

U-Bhf Ernst-
Reuter-Platz



Strasse des 17. Juni



S-Bhf
Tiergarten

Coffee Breaks and Lunch

Lunch is provided to all conference attendees on Monday, Tuesday and Wednesday as well as coffee/tea during all breaks.

Plenary Session

Monday, 19th July 2010

Room MA 041, 8:30-10:10

8:30 **Welcome Addresses**

Chairmen GeMiC 2010

Prof. Dr.-Ing. Georg Böck, Technische Universität Berlin

Frank Henkel, Head of Integrated Circuits and Systems, IMST GmbH

8:50 **Challenges and Thrills in Mobile Phone Development**

Dr. Christoph Kutter, Corporate VP R&D Excellence Infineon Technologies

9:30 **Bio-Medical RFIC**

Dr. Sayfe Kiaei, Professor, Arizona State University

Plenary Speaker 1:

Dr. Christoph Kutter, Corporate VP R&D Excellence, Infineon Technologies

Challenges and Thrills in Mobile Phone Development

Abstract: There were more than 1.1 billion mobile phones sold in 2009 and this number will increase to more than 2 billion cellular devices in 2015. Number wise mobile phones are by far the biggest electronic application and hence bear plenty of challenges and thrills during their development process. The hunger for calculation power is enormously increasing with the new wireless communication standards HSPA, HSPA+ and LTE. Additionally, new features are constantly added into these little smart devices, like MP3-players, cameras, GPS receivers, motion sensors. On the other side, the size of the battery stays constant and operation times of one day and standby times of one week are required. Solving the performance and power trade-off could be easy, if there was not the cost and the form-factor of the device to be considered too. All the components have to fit into a small box of the size of a hand with no more than 100g and should not cost more than a few tens of dollars, depending on the model of the mobile phone.

If there were no problems we would not need engineers – there are plenty of these challenges and thrills in the upcoming years. Good news for our world class engineering team.

About Dr. Christoph Kutter: Dr. Christoph Kutter is Corporate Vice President for R&D Excellence, focusing on R&D effectiveness and efficiency at Infineon Technologies AG in Munich, Germany. Prior to this assignment he headed the development for wireline and wireless products (2004-2009), contributing to the turn-around of the Communications Group.

From 2003 to 2004 he led as Senior Vice President the Infineon Corporate Research, a group working on disruptive innovations. During the same time he was responsible for the R&D Excellence project. From 2001-2002 he acted as a Vice President for Technology & Innovation for Security and Chipcard ICs.

Christoph Kutter started his semiconductor career in 1995 at Siemens AG, as a process development engineer and later as a Department Head of Embedded Flash in Dresden (1997-2000) and Overall Project Leader (2000-2001).

He received the Dipl. Phys. degree from the Technical University Munich in 1992 and the Dr. rer. nat. degree in 1995 from the University of Konstanz, respectively. From 1990 to 1995 he was a research scientist at the High Magnetic Field Laboratory (Max-Planck Institut for Solid State Physics) in Grenoble France.

Plenary Speaker 2:

Dr. Sayfe Kiaei, Professor, Electrical, Energy, and Computer Engineering (ECEE),
Director of Connection One NSF Center, Arizona State University

Bio-Medical RFIC

Abstract: This presentation will be an overview of two recent research projects on Bio-Medical Integrated Circuits at ASU. The first part of the presentation will be an overview of a low power Medical Implantable Communication Services (MICS) transceivers. A Dual band MICS transceiver with a reconfigurable RF front-end is presented. The receiver reuses the same circuit core for I) super-regenerative wake-up receiver, II) receive-mode LNA, and III) transmit power amplifier. The transceiver uses an All Digital Frequency Locked-Loop (ADFLL) for LO signal generation and transmitter's modulation. The device is fabricated in a 0.18 μ m CMOS process. The measured sensitivity of the On-Off Keying (OOK - wakeup receiver) is at -80dBm, while the BFSK receiver's sensitivity is -97dBm with 2mW total power consumption. The nominal output power of the transmitter is -5dBm.

The second part of the presentation will be an overview of a dual-channel directional digital hearing (DHA). The DHA uses MEMS microphones, and an adaptive-power analog processing signal chain. The analog front-end consists of a DDA based capacitance to voltage conversion circuit, 40dB VGA and a power scalable continuous time sigma delta ADC, with 68dB SNR dissipating 67 μ W from a 1.2V supply. The MEMS microphones are fabricated in ASU clean-room using custom MEMS process.

About Dr. Sayfe Kiaei: Dr. Sayfe Kiaei is the Associate Dean of Research at the Ira A. Fulton Schools of Engineering. He has been with ASU since January 2001. He is a Professor and the Director of the Connection One Center (NSF I/UCRC Center), and Motorola Chair in Analog and RF Integrated Circuits. From 1993 to 2001, he was a Senior Member of Technical Staff with the Wireless Technology Center and Broadband Operations at Motorola where he was responsible for the development of RF & Transceiver Integrated Circuits, GPS RF IC, and Digital Subscriber Lines (DSL) transceivers. Before joining Motorola, Dr. Kiaei was an Associate Professor at Oregon State University from 1987-1993 where he taught courses and performed research in digital communications, VLSI system design, advanced CMOS IC design, and wireless systems. Dr. Kiaei assisted in the establishment of the Industry-University Center for the Design of Analog/Digital ICs (CDADIC) and served as a Co-Director of CDADIC for 10 years. He has published over 100 journal and conference papers and holds several patents and his research interests are in wireless transceiver design, RF and Mixed-Signal IC's in CMOS and SiGe. His research projects are funded by a large number of industrial sponsors including Motorola Inc., Intel, the National Science Foundation, Texas Instruments and SRC. He has published more than 75 journal and conference papers and holds several patents. Dr. Kiaei is an IEEE Fellow and a member of IEEE Circuits and Systems Society, IEEE Solid State Circuits Society, and IEEE Communication Society. Dr. Kiaei has been organizer, on the technical program committee and/or chair of many conferences, including: RFIC, MTT, ISCAS, and other international conferences.

Research Interests: Wireless Transceiver Design, RF and Mixed-Signal IC's.

Honors and Distinctions:

Four research awards; Carter Best Teacher Award, Oregon State College of Engineering; IEEE Darlington Award; IEEE Fellow, and Motorola 10X Design award.

IEEE Fellow selection Committee Chair, CAS, IEEE 2009

Ph.D.: Washington State University, 1987

Session 1: Sensor Systems 1

Monday, 19th July 2010

Room MA041

Chair: Roland Thewes, TU Berlin

11:00 **Paper 10008**

P450-Mediated Electrochemical Sensing of Drugs in Human Plasma for Personalized Therapy

Andrea Cavallini¹, Sandro Carrara¹, Victor Erokhin², Giovanni De Micheli¹

¹*Integrated Systems Laboratory - EPFL Lausanne, Switzerland*, ²*CRS SOFT CNR-INFN and Department of physics - Parma University*

11:20 **Paper 10012**

Discharge Characteristics as the Criteria for Replacing Batteries with Power Harvesting Circuits in Sensor Systems

Chomora Mikeka, Hiroyuki Arai

Graduate School of Engineering, Yokohama National University

11:40 **Paper 10017**

An innovative water and ice detection system for monitoring road and runway surfaces

Amedeo Troiano, Eros Gian Alessandro Pasero, Luca Mesin

Dipartimento di Elettronica Politecnico di Torino

12:00 **Paper 10039**

CMOS based biosensor with integrated biomembrane

Sarah Dierk¹, Hoc Khiem Trieu¹, Ingo Kper²

¹*Department Integrated Sensors and Actuators, Fraunhofer IMS Duisburg*,

²*School of Chemistry, Physics and Earth Science, Flinders University, Adelaide*

Session 2: Analog and Mixed Signal Circuits 1

Monday, 19th July 2010

Room MA043

Chair: Thomas Ussmueller, Universität Erlangen-Nürnberg

11:00 **Paper 10035**

Bulk-Driven Flipped Voltage Differential Pair

Yasutaka Haga, Izzet Kale

Applied DSP & VLSI Research Group, School of Electronics and Computer Science, University of Westminster, London

11:20 **Paper 10090**

Limiting Amplifiers for Bits Recovery of Gbps Analog BPSK/QPSK Demodulator

Yinmei Su, Gang Liu, Hermann Schumacher

Institute of Electron Devices and Circuits, Ulm University

11:40 **Paper 10092**

A SiGe 7 Gbit/s Analog BPSK/QPSK Demodulator

Gang Liu, Yinmei Su, Hermann Schumacher

Institute of Electron Devices and Circuits, Ulm University

12:00 **Paper 10097**

Analog design oriented ultra-deep-submicron CMOS technology analysis

Guillaume Pollissard-Quatremère, Geoffroy Gosset, Denis Flandre

Université catholique de Louvain, ICTEAM

12:20 **Paper 10128**

Digital Polyphase Baseband for Direct Digital Generation of High Sample Rate Radio Frequency Signals

Björn Thorsten Thiel, Stefan Dietrich, Renato Negra

Mixed Signal CMOS Circuit, UMIC Research Centre, RWTH Aachen University

Session 3: Sensor Systems 2

Monday, 19th July 2010

Room MA041

Chair: Wolfgang Pribyl, TU Graz

14:00 **Paper 10070**

A Low Power CMOS 0.13 μ m High Dynamic Range Front-End for 100 μ m \times 100 μ m Pixel Sensors

Thanushan Kugathasan

University of Torino and INFN Sezione di Torino

14:20 **Paper 10071**

A Noise Model for Full Characterization of Discrete-Time Current Sensing

Marco Crescentini, Marco Bennati, Marco Tartagni

Advanced Research Center on Electronic Systems (ARCES), University of Bologna

14:40 **Paper 10095**

A microcontrolled neural interface with electrode impedance measurement

Caterina Carboni, Daniela Loi, Gianmarco Angius

Department of Electrical and Electronic Engineering, University of Cagliari

15:00 **Paper 10104**

Multichannel Bipotentiostat System for Cellular Monitoring Platforms

Marco Vergani¹, Marco Carminati¹, Giorgio Ferrari¹, Miriam Adamovski²

¹Dipartimento di Elettronica e Informazione, Politecnico di Milano, ²Institute of Biochemistry and Biology, University of Potsdam

15:20 **Paper 10105**

Very High Density Microelectrode Array with Monolithically Integrated Readout Circuits

Joye Neil¹, Sedigheh Hashemi², Alexandre Schmid¹, Yusuf Leblebici¹

¹Swiss Federal Institute of Technology, EPFL, Lausanne, Switzerland,

²Communication Circuits Laboratory, University of California in Los Angeles

Session 4: Analog and Mixed Signal Circuits 2

Monday, 19th July 2010

Room MA043

Chair: Benjamin Lämmle, Universität Erlangen-Nürnberg

14:00 **Paper 10124**

Hierarchical Performance Estimation of Analog Blocks using Pareto Fronts

Engin Deniz¹, Gunhan Dundar²

¹*Department of Electronic and Communication Engineering, Dogus University,*

²*Department of Electrical and Electronics Engineering, Bogazici University*

14:20 **Paper 10135**

A Novel High Frequency pseudo Noise Correlator Hardware Design for cable fault diagnoses

Holger Geisler, Richard A. Guinee

Department of Electronic Engineering, Cork Institute of Technology

14:40 **Paper 10140**

Digitally-Controlled High-Frequency DC-DC Buck Converter

Ghulam Abbas¹, Cyril Condemine¹, Nacer Abouchi²

¹*University of Lyon, The Lyon Institute of Nanotechnology (INL) University of Lyon, CPE Lyon,* ²*ASIC Design Lab, CEA - LETI MINATEC*

15:00 **Paper 11003**

A Low Bandwidth Pulse-Based Neural Recording System

Sheng-Feng Yen, John G. Harris

Department of Electrical and Computer Engineering, University of Florida

15:20 **Paper 11006**

A Study for Remote Powering of a Knee Prosthesis Through Inductive Link

Oguz Atasoy, Catherine Dehollain

Ecole Polytechnique Fédérale de Lausanne (EPFL)

Session 5: Sensor Systems 3

Monday, 19th July 2010

Room MA041

Chair: Roland Thewes, TU Berlin

16:10 **Paper 10106**

An Analog Closed-Loop SC Accelerometer Interface for a Capacitive High-Q Sensor Element

Mikail Yüçetas, Antti Kalanti, Jarno Salomaa, Lasse Aaltonen, Kari Halonen
SMARAD-2/Electronic Circuit Design Laboratory, Aalto University School of Science and Technology

16:30 **Paper 10132**

A 1-MHz Analog Front-End for a Wireless Bioelectrical Impedance Sensor

Javier Ramos¹, José Luis Ausin¹, Guido Torelli²

¹*Department of Electrical and Electronics Engineering, University of Extremadura*, ²*Department of Electronics, University of Pavia*

16:50 **Paper 10134**

A 3D Image Sensor based on Current Assisted Photonic Mixing Demodulator in 0.18 μ m CMOS Technology

Quazi Delwar Hossain¹, Gian-Frenco Dalla Betta¹, Lucio Pancheri², David Stoppa²

¹*DISI, University of Trento*, ²*Fondazione Bruno Kessler (FBK)*

17:10 **Paper 10146**

3D ranging with a high speed imaging array

Simone Bellisai, Fabrizio Guerrieri, Simone Tisa

Dipartimento di Elettronica ed Informazione, Politecnico di Milano

17:30 **Paper 10149**

Advances in CMOS SoC Radar Sensor for Contact-less Cardiac Monitoring

Martina Mincica^{1,2}, Domenico Pepe¹, Fabio Zito³, Domenico Zito^{1,4}

¹*Tyndall National Institute*, ²*University of Pisa, Dept. of Information Engineering*, ³*University "Mediterranea" of Reggio Calabria, DIMET*, ⁴*University College Cork, Dept. of Microelectronic Engineering*

Session 6: Data Converters

Monday, 19th July 2010

Room MA043

Chair: Eugenio Di Gioia, TU Berlin

16:10 **Paper 10020**
Continuous-Time Delta-Sigma Based Readout Concepts for CZT detector arrays
Matthias Voelker, Haiyan Zhou
Fraunhofer IIS

16:30 **Paper 10031**
A Low Power Time-to-Digital-Converter in 0.13 μ m CMOS with 100ps Time Resolution Capability for Silicon Pixel Radiation Detector
Sara Garbolino, Sorin Martoiu
University of Studies of Turin

16:50 **Paper 10046**
An 8-bit 440-MS/s Pipelined Analog-to-Digital Converter in 0.13-um CMOS
Tero Nieminen, Kari Halonen
Aalto University of Technology, Department of Micro- and Nanosciences

17:10 **Paper 10049**
High-Speed Comparators for SAR ADCs in 130 nm BiCMOS
Johannes Digel¹, Markus Grözing¹, Manfred Berroth¹, Hans Gustat¹, Johann-Christoph Scheytt²
¹Institute of Electrical and Optical Communications Engineering, University of Stuttgart, ²IHP microelectronics

17:30 **Paper 10076**
A 100 Gigabit Measurement System with State of the Art FPGA Technology for Characterization of High Speed ADCs and DACs
Damir Ferenci, Manfred Berroth
Institute of Electrical and Optical Communications Engineering, University of Stuttgart

PRIME Special Session

Tuesday, 20th July 2010

Room MA 041, 8:30-10:10

8:30 **Supporting the European Doctoral Schools: The New EURO-DOTS Support Action of the EC**

Authors: M. Declercq, H.E. Maes, C. Dehollain
Speaker: C. Dehollain

Abstract: The EURO-DOTS (Doctoral Training Support) action is aimed primarily at improving the offer and the quality of training proposed to European PhD students. It helps fulfilling the new requirements for ECTS credits imposed to PhD students by major European universities for obtaining the Doctoral (PhD) degree in Engineering. A coherent set of advanced courses in micro/nanoelectronics explicitly accredited by major European universities in the framework of their Doctoral Program, will be made easily accessible to European PhD students, offering the opportunity to collect ECTS credits thorough Europe. The global objective is to create a delocalized (virtual) platform for supporting the Doctoral Schools in Europe in micro/nanoelectronics. The courses will respect specific organization criteria (short, intensive one-week modules with optional exam) that will make them very flexible, accessible and attractive as well for high-level continuous education of engineers from industry. Scholarships will be made available to PhD students for boosting the start-up of the project, while other sources of scholarships will be explored for the long-term continuation of the project.

About Dr. Catherine Dehollain: Dr. Catherine Dehollain received the degree of electrical engineer in 1982, and the Ph.D. degree in 1995, both from the "Ecole Polytechnique Fédérale de Lausanne", Switzerland (EPFL). From 1982 to 1984, she was a Research Assistant at the Electronics Laboratories (LEG) of EPFL. In 1984, she joined the Motorola European Center for Research and Development, in Geneva, as a Design Engineer. In 1990, she returned to EPFL as a Senior Assistant at the "Chaire des Circuits et Systèmes" (CIRC). She joined the LEG in 1995 as Research Associate. She is the Leader of the RF IC Group (GR-SCI) since 1995. She has been the Project Manager of the Esprit European project SUPREGE, Partner of the IST European projects SODERA, MUMOR, WIDE-RF, MINAMI and NANO-RF. She is the coordinator of the IST European project ULTRASPONDER "In Vivo Ultrasonic Transponder System for Biomedical Applications" and of the Swiss National Funding project (SNF) NEURO-IC "Radio link to record neural activities of the brain. She is partner of the NCCR MICS SNF project "UWB localization for small robots" and of the Nano-Tera SNF projects SIMOS, I-Ironic and Placitus, dedicated to wireless communication for biomedical applications. Since 1998, she has been a Lecturer at EPFL in the area of radio frequency circuits, electric filters and CAD tools. Since 2006, she is "Maitre d'Enseignement et de Recherche" (MER) at EPFL. Her technical interests include low-power analog circuits, biomedical remotely powered sensors, and electric filters. She is an author or co-author of four scientific books and 55 articles.

PRIME Special Session - continued

9:00 **Company presentation: Rohde & Schwarz**
Dr. Wolfram Titze

9:10 **Company presentation: Computer Simulation Technology – CST**
Dr. Tilmann Wittig

9:20 **Company presentation: Ansys**
Dr. Devin Crawford

9:30 **Company presentation: IMST GmbH**
Frank Henkel

9:40 **Company presentation: Agilent**
Gilbert Berger

9:50 **Company presentation: Broadcom Netherlands B.V.**
Davide Vecchi

10:00 **Company presentation: Intersil**
Dr. Peter Mole

Session 7: Low Noise Amplifiers

Tuesday, 20th July 2010

Room MA041

Chair: Renato Negra, RWTH Aachen

11:00 **Paper 10040**

Comparison of Various 2.4GHz LNA Topologies

Alena Djugova, Jelena Radic, Mirjana Videnovic-Misic

Department of Power, Electronics and Communications Engineering, Faculty of Technical Sciences, University of Novi Sad

11:20 **Paper 10042**

Design Experiences of a CMOS LNA for mm-waves

Enrique Rivera, Cyril Botteron, Pierre-André Farine

Ecole Polytechnique Fédérale de Lausanne (EPFL), Electronics & Signal Processing Laboratory

11:40 **Paper 10065**

A Discrete-Components Impulse-Radio UWB Low-Noise Amplifier with Voltage Controlled-Gain

James Colli-Vignarelli, Catherine Dehollain

Ecole Polytechnique Fédérale de Lausanne - STI RFIC group

12:00 **Paper 10093**

Fully differential low-noise amplifier with offset reduction for high-resolution neural signal recording

Urs Alexander Müller, Steve Tanner, Pierre-André Farine

Electronics and Signal Processing Laboratory, EPFL, Switzerland

Session 8: Image Processing

Tuesday, 20th July 2010

Room MA043

Chair: Peter Kennedy, University College Cork

11:00 **Paper 10061**

Optimized Parallel Implementation of Pedestrian Tracking Using HOG Features on GPU

Hiroki Sugano¹, Ryusuke Miyamoto², Yukihiro Nakamura³

¹*Dept. of Comm. and Computer Eng., Kyoto University*, ²*Dept. of Information Systems, Nara Institute of Science and Technology*, ³*Research Org. of Science and Eng., Ritsumeikan University*

11:20 **Paper 10139**

Practical Single-Byte Fault Injection Techniques by Laser on an AES Cryptosystem

Jean-Max Dutertre¹, Amir-Pasha Mirbaha¹, David Naccache², Assia Tria³

¹*École Nationale Supérieure des Mines de Saint-Étienne (ENSMSE)*, ²*Équipe de Cryptographie, École Normale Supérieure, Paris*, ³*CEA-LETI, Gardanne, France*

11:40 **Paper 10142**

Application of Partial Reconfiguration of FPGAs in Image Processing

Tamás Raikovich, Béla Fehér

Department of Measurement and Information Systems, Budapest University of Technology and Economics

Session 9: Power Amplifiers and Power Devices

Tuesday, 20th July 2010

Room MA041

Chair: Chafik Meliani, Ferdinand-Braun-Institut Berlin
Claudio Collura, Intersil GmbH

14:00 **Paper 10041**

Energy Capability Improvement of Large DMOS Transistors by Adaptive Current Redistribution

Martin Pfost, Dragos Costachescu

Infineon Technologies Romania

14:20 **Paper 10060**

Fully Monolithically Integrated X-Band Power Amplifier without External Matching

Ievgenii Meshcheriakov, Valentyn A. Solomko, Peter Weger

Chair of Circuit Design, Technical University of Brandenburg

14:40 **Paper 10074**

A 24GHz CMOS Digitally Modulated Polar Power Amplifier with Embedded FIR Filtering

Hyungseok Kim, Tino Copani, Sayfe Kiaei

School of Electrical, Computer and Energy Engineering, Arizona State University

15:00 **Paper 10143**

A 1.7 GHz-to-3.1 GHz fully integrated broadband class-E power amplifier in 90 nm CMOS

Danish Kalim, Denis Erguvan, Renato Negra

Mixed Signal CMOS Circuits, UMIC Research Centre, RWTH Aachen University

Session 10: Analog and Digital Signal Processing

Tuesday, 20th July 2010

Room MA043

Chair: Peter Kennedy, University College Cork

14:00 **Paper 10067**

Acquisition Performance of Galileo E5a Signal

Youssef Tawk, Cyril Botteron, Aleksandar Jovanovic, Pierre-André Farine
Ecole Polytechnique Fédérale De Lausanne, Institute of Microengineering (IMT)

14:20 **Paper 10079**

On the key schedule of Mini-AES Algorithm

Rashmi Ramesh Rachh¹, Pemmaraju. V. Ananda Mohan², Basavraj S Anami³
¹Department of Computer Science, KLE college of Engineering and Tech, Belgaum, India, ²R & D Division, ³KLE Institute of Technology, Hubli, India

14:40 **Paper 10083**

Implementation of Realtime Pipeline-Folding 64-Tap Filter on FPGA

Pongyupinpanich Surapong¹, Manfred Glesner¹, Harald Klingbeil²
¹Institute of Microelectronic Systems, Darmstadt University of Technology, ²Gesellschaft für Schwerionenforschung mbH, Darmstadt, Germany

15:00 **Paper 10110**

Sound Recognition with Spiking Silicon Cochlea and Hidden Markov Models

David Jäckel¹, Rico Moeckel², Shih-Chii Liu²
¹Bio Engineering Laboratory, Dept. of Biosystems Science and Engineering, ETH Zürich, ²Institute of Neuroinformatics, Institute of Neuroinformatics, University of Zürich and ETH Zürich

Session 11: Poster Session

Tuesday, 20th July 2010

Foyer – First Floor

Chair: Viswanathan Subramanian, TU Berlin
Daniel Gruner, TU Berlin

Paper 10010

Digital Shaping of Static and Dynamic Mismatch Errors in Digital to Analog Converters

Bastian Mohr¹, Niklas Zimmermann¹, Björn Thorsten Thiel², Renato Negra², Stefan Heinen¹

¹Chair of Integrated Analog Circuits, RWTH Aachen University, ²Mixed-Signal CMOS Circuits, RWTH Aachen University

Paper 10024

An Innovative Transition Method to Reduce Conducted Emissions for Automotive High Side Power Switch

Laurentiu Ovidiu Creosteanu, Gheorghe Brezeanu

University "POLITEHNICA" Bucharest, Electronics, Telecommunication and IT Faculty

Paper 10029

Lateral Drift-Field Photodetector for High Speed 0.35µm CMOS Imaging Sensors Based on Non-Uniform Lateral Doping Profile: Design, theoretical concepts, and TCAD Simulations

Rana Mahdi, Johannes Fink, Bedrich J. Hosticka

Department of Optical Sensor Systems, Fraunhofer Institute for Microelectronic Circuits and System (IMS) Duisburg, Germany

Paper 10048

Effect of Capacitance on the Output Characteristics of Solar Cells

Patrick Merhej, Enrico Dallago, Daniele Finarelli

Department of Electrical Engineering, University of Pavia, Italy

Paper 10053

On the Use of Black Silicon Obtained by Reactive Ion Etching as the Hot Spot of a Thermoelectric Generator Heated by Electromagnetic Radiation

Ngoc Kim Nguyen¹, Elodie Richalot², Philippe Basset¹

¹Université Paris-Est, ESYCOM, ESIEE Paris, ²Université Paris-Est, ESYCOM, Université de Marne-la-Vallée Champs-sur-Marne

Paper 10062

FPGA based ASIC fast prototyping system for new generation piezo injectors control units

Simone Alpe, Gianluca Botto, Mirko De Giuseppe

Mechatronics Laboratory – Politecnico di Torino

Paper 10064

Automatic Assembler Generator for NoGAP

Per Karlström, Sumathi Logonathan, Faisal Akhlaq, Dake Liu

Department of EE, Linköping University

Paper 10087

A Digital Calibration Scheme for Low-Power Multi-Bit Pipeline ADCs

Tamin Faiq¹, Olujide Adeniran², Andreas Demosthenous¹

¹*Department of Electronic and Electrical Engineering, University College London,* ²*Mircs Semiconductor*

Paper 10099

A 1-V 225-nW 1KS/s Current Successive Approximation ADC for Pacemakers

Salim K Al-Ahdab, Reza Lotfi, Wouter A Serdijn

Delft University of Technology, the Netherlands

Paper 10103

Automatic mutli-connectivity interface generation for system designs based on a dataflow description

Richard Thavot, Ab Al-Hadi Bin Ab Rahman, Romuald Mosqueron, Marco Mattavelli

Ecole Polytechnique Fédérale de Lausanne, GR-SCI-MM

Paper 10112

Automatic Impedance Matching in Microwave Power Harvesters

Ping Zhao, Yuliang Zheng, Manfred Glesner

Darmstadt University of Technology

Paper 10113

Current conveyor circuit improvement

Lukas Burian, Pravoslav Martinek

Department of Circuit Theory, Faculty of Electrical Engineering, Czech Technical University in Prague

Paper 10115

Integrated Temperature Compensation Scheme for a Standard Linear CMOS Vision Sensor

Hakim Zimouche, Gilles Sicard

TIMA Laboratory, CNRS - Grenoble INP - UJF

Paper 10123

A high output voltage swing logarithmic image sensor designed with on chip FPN reduction

Hawraa Amhaz, Gilles Sicard

TIMA Laboratory, CNRS - Grenoble INP - UJF

Paper 10130

Delta Sigma ADC design flow through a Labview based design and benchmarking tool: architecture mapping

Francesco Rizzo^{1,3}, Domenico Zito², Roberto Saletti¹, Rolf Becker³

¹Dept. of Information Engineering, University of Pisa, ²Dept. of Microelectronic Engineering, University College Cork and Tyndall National Institute, ³Cellular Systems & Connectivity Group, ST-Ericsson

Paper 11005

Hardware and Software Synthesis of Image Filters From CAL Dataflow Specification

Ab Al-Hadi Ab Rahman¹, Richard Thavot¹, Marco Mattavelli¹, Pascal Faure²

¹Ecole Polytechnique Fédérale De Lausanne, ²AKAtech SA

Session 12: Device Technology and Passives

Tuesday, 20th July 2010

Room MA041

Chair: Wolfgang Heinrich, Ferdinand-Braun-Institut Berlin

16:10 **Paper 10032**

Study of Proximity-Coupling: Application to new RF-Interconnects

Constant Mombo Boussougou, Thierry Le Gouguec, Yves Quéré, Fabrice Huret
Université Européenne de Bretagne, France

16:30 **Paper 10033**

Properties of Source-Gated Transistors in Polysilicon

Radu Alexandu Sporea, John M. Shannon, S. Ravi P. Silva
Advanced Technology Institute, Faculty of Electronics and Physical Sciences, University of Surrey

16:50 **Paper 10052**

Development of vertical superlattices in silicon for on-chip thermal management

Jayalakshmi Parasuraman¹, Mathieu Bardoux², Philippe Basset¹
¹Laboratoire ESYCOM, ESIEE, Université Paris-Est, ²MATEIS, UMR-5510 CNRS, Université Lyon 1, INSA de Lyon

17:10 **Paper 10119**

Power-Gating: More Than Leakage Savings

Andrea Calimera, Enrico Macii, Massimo Poncino
Politecnico di Torino

17:30 **Paper 10122**

Modeling of MIM Capacitors in 0.25 μ m SiGe BiCMOS Process up to 140 GHz

Amin Hamidian, Zihui Zhang, Viswanathan Subramanian, Georg Boeck
Microwave Engineering Laboratory, Berlin Institute of Technology

Session 13: Computer Aided Design

Tuesday, 20th July 2010

Room MA043

Chair: Frank Henkel, IMST GmbH

16:10 **Paper 10027**

Development of an Innovative Electrolytes Characterization Approach using a Combined COMSOL/MATLAB/HSPICE System

Matteo Scaramuzza, Alberto Ferrario, Alessandro De Toni

Department of Electronic Engineering, University of Padua

16:30 **Paper 10069**

Rational modeling of interconnect networks using multi-parameter Kautz functions

Nadia Iassamen, Mihai Telescu, Pascale Bréhonnet, Noël Tanguy

Université Européenne de Bretagne

16:50 **Paper 10078**

Overview of an environment for automated electrical behaviour modelling using data-based methods

Philipp Senger¹, Rolando Dölling¹, Wolfgang Rosenstiel²

¹Robert Bosch GmbH, ²University of Tuebingen, Department of Computer Engineering

17:10 **Paper 10081**

FPGA-Based Acceleration of the AutoDock Molecular Docking Software

Imre Pechan¹, Béla Fehér¹, Attila Bérces²

¹Department of Measurement and Information Systems, Budapest University of Technology and Economics, ²Chemistry Logic Ltd.

17:30 **Paper 10091**

IN-VEHICLE COMMUNICATION NETWORK STATISTICAL ANALYSIS USING VHDL-AMS BEHAVIORAL MODELS

Candice Muller, Maurizio Valle

DIBE - Biophysical and Electronics Engineering Department, University of Genoa

Session 14: Transceivers

Wednesday, 21th July 2010

Room MA041

Chair: Tobias Werth, RWTH Aachen

08:50 **Paper 10018**

Ultra-Wideband Transmitters based on M-Sequences for High Resolution Radar and Sensing Applications

Benjamin Sewiolo, Benjamin Laemmle, Robert Weigel

Institute for Electronics Engineering, University of Erlangen-Nuremberg

09:10 **Paper 10055**

Design of Received Signal Strength Indicators for RF-MIMO Systems

Uwe Mayer, Michael Wickert, Frank Ellinger

Chair for Circuit Design and Network Theory, Dresden University of Technology

09:30 **Paper 10126**

System simulation of Adaptive I/Q Mismatch Compensation method using SystemC-AMS

Yifan Wang, Zhimiao Chen, Christoph van Meersbergen, Stefan Heinen

Chair of Integrated Analog Circuits, RWTH Aachen university

09:50 **Paper 10136**

Low Power Multi-band CMOS Receiver Front-End

Kittichai Phansathitwong, Henrik Sjöland, Pietro Andreani

Dept. of Electrical and Information Technology, Lund University

10:10 **Paper 10137**

Modelling and simulation of an RF-DAC based transmitter at architectural level in SystemC/AMS

Junqing Guan, Renato Negra

Mixed-Signal CMOS Circuits, UMIC Research Centre, RWTH Aachen University

Session 15: Digital and Low Power Circuits

Wednesday, 21th July 2010

Room MA043

Chair: Tim Hollis, Micron Technology, Inc.

08:50 **Paper 10023**

A Timing Error Detection Latch Using Subthreshold Source-Coupled Logic

Matthew J. Turnquist¹, Erkka Laulainen¹, Jani Mäkipää², Lauri Koskinen¹

¹*Electronic Circuit Design Laboratory Aalto School of Science and Technology,*
²*VTT National Research Centre of Finland*

09:10 **Paper 10037**

Feasibility study of partial-RESET Multilevel programming in Phase Change Memories

Stefania Braga, Alessandro Sanasi, Alessandro Cabrini, Guido Torelli

University of Pavia, Department of Electronics

09:30 **Paper 10050**

Efficient Architecture for High-Speed Low-Power SC SD Modulators

Francesco Antonio Amoroso, Gregorio Cappuccino, Andrea Pugliese

Department of Electronics, Computer Science and Systems, University of Calabria

09:50 **Paper 10108**

A Dynamically Reconfigurable Architecture for Vision Pre-processor

Bin Zhang, Kuizhi Mei

Institute of Artificial Intelligence and Robotics, Xi'an Jiaotong University

10:10 **Paper 10131**

Impact of Dual Placement on WDDL Design security in Mesh-Based and Tree-Based FPGAs

Emna Emna Amouri, Zied Marrakchi, Habib Mehrez

LIP6, Universite Pierre et Marie Curie

Session 16: Frequency Synthesizers

Wednesday, 21th July 2010

Room MA041

Chair: Catherine Dehollain, Ecole Polytechnique Fédérale de Lausanne

11:00 **Paper 10016**

A Nested Digital Delta-Sigma Modulator Architecture for Fractional-N Frequency Synthesis

Brian Fitzgibbon¹, Michael Peter Kennedy¹, Franco Maloberti²

¹Department of Microelectronic Engineering and Tyndall National Institute, University College Cork, ²Department of Electronics, University of Pavia

11:20 **Paper 10019**

An Ultra Low-Power CMOS Frequency Synthesizer for Low Data-Rate sub-GHz Applications

Calogero Marco Ippolito, Alessandro Italia, Giuseppe Palmisano

Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi, Università di Catania, Facoltà di Ingegneria, DIEES

11:40 **Paper 10044**

Continuous Gain Calibration of an FM-Radio Transmitter based on an All-Digital PLL

Jan Henning Mueller, Andreas Neyer, Ralf Wunderlich, Stefan Heinen

Chair of Integrated Analog Circuits and RF Systems, RWTH Aachen University

12:00 **Paper 10086**

Analysis of Thermal Noise and the Effect of Parasitics in the Charge-Pump Integrator

Alireza Nilchi, David A. Johns

Electrical and Computer Engineering, University of Toronto

12:20 **Paper 10141**

A Describing Function Based Method for Predicting the Stability of Higher-Order High-Pass Sigma-Delta Modulators

Gunes Damla Altinok, Mohammed Al-Janabi, Izzet Kale

Applied DSP and VLSI Research Group, Department of Electronics, University of Westminster, London

Session 17: VLSI

Wednesday, 21th July 2010

Room MA043

Chair: Tim Hollis, Micron Technology, Inc.

11:00 **Paper 10005**

Estimating IC Self-Heating for on-Wafer Measurements

Stefan Hauptmann, Christian Knochenhauer, Michael Wickert, Frank Ellinger

Chair for Circuit Design and Network Theory, Dresden University of Technology

11:20 **Paper 10082**

TDM Switch-based Crossbar Architecture

Pongyupinpanich Surapong, Manfred Glesner

Institute of Microelectronic Systems, Darmstadt University of Technology

11:40 **Paper 10084**

Fault Resilient Intra-die and Inter-die Communication in 3D Integrated Systems

Vladimir Pasca, Lorena Anghel, Mounir Benabdenbi

TIMA Laboratory, Grenoble, France

Session 18: Frequency Generation/Conversion Circuits

Wednesday, 21th July 2010

Room MA041

Chair: Dzianis Lukashevich, Intersil GmbH

14:00 **Paper 10007**

An Automatic Retiming System for Asynchronous Fractional Frequency Dividers

Davide Tasca, Marco Zanuso, Salvatore Levantino, Carlo Samori

Dipartimento di Elettronica e Informazione, Politecnico di Milano

14:20 **Paper 10009**

Fully Integrated 50MHz Frequency Reference with 1ppm Absolute Accuracy within 0-80C

Erdogan Ozgur Ates, Devrim Yilmaz Aksin

Electrical and Electronics Engineering Faculty, Istanbul Technical University

14:40 **Paper 10015**

Quadrature Frequency Divider with Programmable Duty Cycle

Tobias D. Werth, Florian de Sordi, Stefan Heinen

Chair of Integrated Analog Circuits and RF Systems, RWTH Aachen University

15:00 **Paper 10054**

Analysis of Forward Body Biasing (FBB) in a Complementary Differential LC Injection-Locked Frequency Divider based on Direct Injection

Saeid Daneshgar, Michael Peter Kennedy

Department of Microelectronic Engineering and Tyndall National Institute, University College Cork

15:20 **Paper 10121**

Comparison of VCO Topologies

Michael Haase, Viswanathan Subramanian, Tao Zhang, Amin Hamidian

Microwave Engineering Lab, Berlin Institute of Technology

Session 19: Sigma Delta Modulators

Wednesday, 21th July 2010

Room MA043

Chair: Franco Maloberti, University of Pavia

14:00 **Paper 10026**

Hardware Reduction in Higher Order MASH Digital Delta-Sigma Modulators via Error Masking

Brian Fitzgibbon, Michael Peter Kennedy

Department of Microelectronic Engineering and Tyndall National Institute, University College Cork

14:20 **Paper 10045**

Design of Continuous-Time Sigma Delta Modulators with Real Analog Blocks

Oscar Belotti, Franco Maloberti

Department of Electronics, University of Pavia

14:40 **Paper 10066**

A Reconfigurable Integrated Transmission Line Sigma Delta Modulator for the UWB/WLAN Receiver

Ali Zahabi, Muhammad Anis, Maurits Ortmanns

Institute of Microelectronics, University of Ulm

15:00 **Paper 10080**

Parallelization of Bandpass Sigma-Delta Modulators for Class-S Digital Power Amplifiers

Tomasz Podsiadlik, John Dooley, Ronan Farrell

Centre for Telecommunications Research, National University of Ireland

15:20 **Paper 10094**

Multibit continuous-time sigma-delta modulator with reduced number

Julian Garcia, Ana Rusu

School of Information and Communication Technology (ICT), Royal Institute of Technology (KTH)

Workshops

Rohde & Schwarz

Tuesday, 20th July 2010, 10:40 – 11:30

Room MA141

Working for Rohde & Schwarz - the international communications engineering company with challenging tasks for engineers

Rohde & Schwarz is an independent leading supplier of solutions in the fields of test and measurement, broadcasting, radiomonitoring and radiolocation as well as secure communications. This presentation will introduce the company and its various fields of business. With development facilities in various countries across the world, R&S is an attractive employer for electrical, communications, radio frequency, microwave and computer engineers. The second part of the presentation will illustrate the interesting challenges an engineer has to tackle during product development using the development of the BBA100 broadband amplifier as a case study – a taste of what it is like to work in industry. Finally, employment opportunities at Rohde & Schwarz will be discussed.

CST - Computer Simulation Technology

Tuesday, 20th July 2010, 11:30 – 12:20

Room MA141

Virtual Prototyping based on 3D Electromagnetic Simulation for Advanced Microelectronic Systems

With continuously increasing packing densities and at the same time increasing operating frequencies, electromagnetic effects become more and more pronounced in microelectronics and packaging, which need to be considered in early design stages already. Classical approaches based on Kirchhoff's equations or other simplified formulations typically may not predict this behavior accurately anymore for modern systems.

During this presentation the full-wave 3D simulation tool CST MICROWAVE STUDIO® will be presented for different applications in the world of microelectronics. After a short introduction in the various available simulation technologies used (e.g. time and frequency domain solvers as well as the intuitive import of package data), a number of relevant examples will be shown covering topics such as the design of passive components in radio frequency system-in-a-package (RF SIP), e.g. 3D helical inductors, vertically interdigitated capacitors (VICs), 3D filters, antennas, signal and power integrity questions and finally EMC issues. 3D EM simulation allows a virtual prototyping long before the first physical prototype may fail, in addition it allows insight in the functionality of a system which are not accessible by measurement procedures.

Agilent

Tuesday, 20th July 2010, 13:40 -15:20

Room MA141

High Speed Digital Design - Gigabit Eye Diagrams in Seconds

The continuously increasing data rates on digital data buses such as routers, servers, mass storage systems, and PCs sets a new level of complexity for the hardware designer in terms of signal integrity issues. At multigigabit per second data rates and with channel flight times longer than a bit period, signal integrity is a further major concern. Under these conditions, high-speed analog effects, previously only seen in high frequency RF and microwave engineering, can impair the signal quality and degrade the bit error rate of the link. The new "Channel Analyzer Technology" enables the high speed digital designer to simulate, optimize and verify a high speed digital transmission channel design in seconds. Analyzing complete serial links by co-simulating individual components, each at its most appropriate level of abstraction such as link-, circuit- or physical-level. The output shows the performance of the serial link in form of eye diagrams, statistical BER-Eye Contours, BER-Bathtub over Time and Voltage in a very short time and an extreme advanced jitter analysis.

MMIC- and RFIC Design - Different technologies need different design flows.

GaAs, SiGe and CMOS are the main technologies for MMIC/RFIC design. Advanced and unique simulation algorithms enable full characterization of complete transceivers prior to tape-out. Frequency- and time-domain simulation techniques are used to accurately simulate the complex MMIC/RFIC- Wireless design performance. Yield Analysis and Design Verification by applying wireless standards is the key of success to ensure device manufacturability and reduce design spins. This speech will discuss the different approaches and how the Agilent EESof tools fit into the appropriate design flow.

Advanced RFIC design tools for the Cadence based design flow

CMOS and SiGe RFIC design in the 24 GHz, 60 GHz and higher are not seldom today and will be used in more applications in the future. To solve the RF problems real expert tools and RF focused analyzes are needed. This speech will give an overview of the state of the art RFIC design tools from Agilent EESof plugged in into the Cadence design flow. Circuit simulation, powerful statistical analyzes, all fully integrated in the Cadence ADE. Integrated EM tools in Virtuoso allow precise coil modeling, layout and package effects without leaving the design environment or a transfer into another tool.

Advanced MMIC design tools for ADS based design flow

GaAs is the basis material for MMICs which operate in most high-frequency range for wireless and high-speed electronic products, performing functions such as microwave mixing, power amplification, low noise amplification, and high frequency switching. Advanced Design System (ADS) enables the RF-Engineer to complete the MMIC design without leaving the ADS Design environment. Schematic to Layout and Layout to Schematic synchronization, integrated EM simulators such as MoM and FEM, DRC, LVS, Design of experience (DOE), Yield optimization and Verification applying Wireless test benches enables a first pass of the prototype.

Ansys

Wednesday, 21st July 2010, 8:30 – 10:10

Room MA141

Electromagnetic Simulation for Signal Integrity, Power Integrity and Electromagnetic Compatibility

The problem of electromagnetic compatibility has historically been relegated to the domain of the experimentalist. Systems that are affected by such problems are exceedingly complex, and the EMC phenomena are often not well understood. Sources and the propagation mechanism responsible for EMC are often determined only after detailed measurements that occur late in the design cycle. Consequently, EMC issues may have significant impact on development costs and schedules. Conversely, the related topics of signal integrity and power integrity are often addressed using simulation early in the design cycle.

Extensive use of electromagnetic simulation to understand and optimize power distribution networks and signal integrity has solidified confidence in the accuracy and utility of predictive simulation early in the design cycle. The main impediment to applying these techniques to larger complex systems is the high demand on computing resources. It is well known, however, that CPU speed, power efficiency and built in memory have continued to improve at an exponential rate. Also, new algorithms have been implemented to more efficiently solve electromagnetic phenomena using numerical methods.

This talk will describe the current state of the art in electromagnetic simulation and how simulation is used to optimize electronic systems with respect to signal and power integrity. Additionally, aspects of power integrity and signal integrity that are directly related to EMC will be described in detail. It will be shown how recent advances in hybrid solver technology can be used to predict EMC behavior of complex electronic systems.

Closing Session

Wednesday, 21st July 2010

Room MA041, 15:20-16:20

15:20 **Awards Ceremony**
Invitation to PRIME2011
Closing Remarks

Social Events

PRIME 2010 Welcome Reception

Monday, 19th July 2010

Foyer – First Floor, Mathematics Building

Starting at 17:30

After the first day of PRIME2010, the attendees are invited to attend the welcome reception. It will take place at the conference venue after the end of PRIME sessions on Monday, July 19th. The reception includes drinks, food and entertainment.

PRIME 2010 City Tour

Tuesday, 20th July 2010, 20:00 (Departure!)

Salzufer, close to the Mercedes building

A special treat awaits you, if you registered for the city tour. While gliding on the river Spree, you will see many of the famous sight-seeing spots Berlin has to offer. During the boat ride food and drinks will be offered, which means you can really look forward to a very pleasant evening.

We kindly ask you not to forget the ticket which you will receive during the conference registration.

